REMARKS

The application has been carefully reviewed in light of the Office Action dated February 5, 2004. Claims 4, 18, 32 and 44 have been canceled without prejudice. Claims 1, 15, 29, 33, 41, 49, 50 and 51 have been amended. Claim 52 has been newly added. Claims 1, 2, 5, 6, 10-13, 15, 16, 19, 20, 24-27, 29, 30, 33, 34, 38-43, 45-47 and 49-52 remain pending in this case.

Claims 1, 2, 4-6, 10-13, 15, 16, 18-20, 24-27, 29, 30, 32-34, 38-47 and 49-51 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants' admitted prior art (AAPA) in view of Ashuri (U.S. Patent No. 5,652,530). Applicants respectfully traverse the rejection and request reconsideration.

Claims 4, 18, 32 and 44 have been canceled, and therefore, the rejection is no longer applicable to those claims.

Amended claims 1, 15, 29 and 49-51 each recite a plurality of output circuits each of which outputs a respective data signal, a clock source and a plurality of adjustable delay circuits for receiving a first clock signal and for providing a respective delayed first clock signal to a respective one of said plurality of output circuits, "wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the first clock signal [. . .] such that each of said respective data signals is output by said plurality of output circuits at substantially the same time."

Claim 41 recites receiving a plurality of data output signals, providing a first clock signal, generating respective applied clock signals and adjusting the delay of each of said respective applied clock signals such that the data output signals are output from . . . respective outputs of said output circuits at substantially the same time."

Neither AAPA nor Ashuri teach or suggest the above-described limitations of claims 1, 15, 29 and 49-51.

For example, while Ashuri appears to disclose clock shifting in an individual digital integrated circuit to account for different amounts of propagation delay (e.g., due to different amounts of logic circuits encountered) for a given data signal (See Ashuri at FIG. 3 and Abstract), Ashuri does not teach or suggest a plurality of adjustable delay circuits wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to a first clock signal such that a plurality if data signals are output by a respective plurality of output circuits at substantially the same time.

At best Ashuri could be taken to suggest that e.g., three integrated circuits that require three different clock delay times, due to the respective amounts of logic circuits introduced in their respective data paths, will clock out data at three different times because Ashuri merely ensures that a particular internal clock signal of a respective integrated circuit is delayed to match its own internal data signal. For example, if a first circuit requires a one second delay of its clock signal to correspond to the timing delay of its data signal, a second circuit requires a five second delay of its clock signal to correspond to the timing delay of its data signal, and a third circuit requires a ten second delay of its clock signal to correspond to the timing delay of its data signal, nowhere does the combination of Ashuri or AAPA teach or suggest that the data signals are output from all three integrated circuits at substantially the same time, as defined by claims 1, 15, 29, 41 and 49-51. Rather, one would expect that the output signals would be output at three different times. At least for these reasons, claims 1, 15, 29, 41 and 49-51 are allowable over Ashuri and AAPA.

Claims 2, 5, 6, 10-13, 16, 19, 20, 24-27, 30, 33, 34, 38-40, 42, 43, 45-47 and new claim 52 depend from claims 1, 15, 29 and 41 and are allowable at least for the reasons mentioned above in connection with claims 1, 15, 29 and 41 and also on their own merit.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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